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G11C 14/00**G11C 11/22****H01L 27/10****H01L 21/8247****H01L 29/788****H01L 29/792**(21) Application number: **07064317**(71) Applicant: **SONY CORP**(22) Date of filing: **23.03.95**(72) Inventor: **EMORI TAKAYUKI**(54) **FERROELECTRIC MEMORY**

(57) Abstract:

PURPOSE: To obtain a ferroelectric memory which can surely perform erasure- blocking operation for a non-selection cell in data erasing operation.

CONSTITUTION: A gate oxide film 5, the lower part electrode 4, a ferroelectric film 3, and the upper part electrode 2 are formed in this order in a channel region formed between a source 6 and a drain 7. In data erasing operation, voltage 0V is impressed to a silicon substrate 8 continuously. Negative voltage '-Vpp' is impressed to the upper part electrode 2 of a selection cell with the prescribed fall timing, thereby, the ferroelectric film 3 is polarized in the prescribed one side direction, and memory data is erased. Voltage 0V is continuously impressed to the upper part electrode 2 of a non-selection cell, and a polarization state of the ferroelectric film 3 is held as it is.

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